REMARKS

In view of the above amendments and the following remarks, reconsideration of the objections and rejections set forth in the Office Action of March 9, 2005 is respectfully requested.

In order to make necessary editorial corrections, the entire specification and abstract have been reviewed and revised. As the revisions are quite extensive, the amendments to the specification and abstract have been incorporated into the attached substitute specification and abstract. For the Examiner's benefit, a marked-up copy of the specification indicating the changes made thereto is also enclosed. No new matter has been added by the revisions. Entry of the substitute specification is thus respectfully requested.

On page 2 of the outstanding Office Action, the Examiner objected to originally-pending claims 1-10 due to various informalities. However, as indicated above, all of the original claims have now been cancelled and replaced with new claims 11-35. The new claims have been drafted so as to address all of the Examiner's objections, and so as to place the original claims in a proper form according to U.S. practice. Consequently, it is respectfully submitted that the Examiner's objections to the original claims are not applicable to the new claims.

On pages 3 and 4 of the outstanding Office Action, the Examiner rejected claims 1-3 as being anticipated by the Enomoto reference (US Application Publication 2003/0032284 A1); and rejected claims 5, 6, and 10 as being unpatentable over the Enomoto reference. However, on page 5 of the outstanding Office Action, the Examiner also indicated that dependent claims 4 and 7-9 contain allowable subject matter. Thus, the original claims have now been cancelled, and a set of new claims has been submitted. For the reasons discussed below, it is respectfully submitted that the new claims are clearly patentable over the prior art of record.

New independent claim 1 has been drafted to include all of the subject matter of original base independent claim 1 and allowable dependent claim 4; new independent claim 18 has been drafted to include all of the subject matter of original base independent claim 1 and allowable dependent claim 7; new independent claim 24 has been drafted to include all of the subject matter of original base independent claim 1 and allowable dependent claim 8; and new

independent claim 31 has been drafted to include all of the subject matter of original base independent claim 1 and allowable dependent claim 9. Therefore, in view of the Examiner's indication of allowable subject matter, it is respectfully submitted that independent claims 11, 18, 24, and 31, and the claims that depend therefrom, are clearly patentable over the prior art of record.

In view of the above amendments and remarks, it is submitted that the present application is now in condition for allowance. However, if the Examiner should have any comments or suggestions to help speed the prosecution of this application, the Examiner is requested to contact the Applicant's undersigned representative.

Respectfully submitted,

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Version with Markings to Show Changes Made

METHOD OF MANUFACTURING SEMICONDUCTOR ELEMENT

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The present invention relates to a method of manufacturing a semiconductor element, and especially a semiconductor element~~,~~ which has metallic silicide layer in its gate electrode.

Description of the Related Art

[0002] As high integration of semiconductor devices proceeds, a demand for faster and finer elements of semiconductors increases. To meet ~~accept~~ this demand, a gate electrode comprising a metallic silicide layer is adopted for a semiconductor element of MOS structure.

[0003] A gate electrode having a metallic silicide layer is formed, for example, as described below.

[0004] At first, an isolation of an element is performed. After this, a gate oxide film and a polysilicon film are formed, in this order. Then, a metallic silicide layer is formed on the polysilicon film by a PVD method or a CVD method. A ~~And, a~~ SiN layer is formed on ~~the~~ top of the gate electrode with a thermal process using CVD of reduced pressure etc. This thermal process is performed at a comparatively high temperature in ~~of~~ a range of 700° C to 800° C.

[0005] After forming in ~~a~~ SiN layer, a lithography for forming a gate electrode is performed. In addition~~And~~, an etching process for forming a gate electrode is performed with this patterned SiN layer used as a mask. Thus, a gate electrode is formed. After ~~And, after~~ this, the photo-resist used for etching is removed.

[0006] After removing the photo-resist, oxide films are formed for covering the side walls of the gate electrode with a CVD method of reduced pressure etc.

[0007] However, the conventional structure of the gate electrode mentioned above could not sufficiently recover from the damage received during the etching process, because ~~for~~ the side wall of the gate electrode was covered with oxide film by a CVD method of reduced pressure. This ~~And, this~~ is a problem to be solved. Moreover, over-etching of the gate oxide film occurs. Consequently~~And, by this~~, it becomes impossible to compensate for thinning of the gate oxide film. As a result, there was another problem of causing leakage ~~leak~~ of the gate.

[0008] Therefore, in order to prevent ~~leak~~ leakage of the gate, a method of performing heat oxidation treatment is generally used. But, in the method mentioned above, a heat treatment for forming SiN layer was necessary. Therefore, the metallic silicide was crystallized, and~~. And~~, the crystal was in a state that oxygen was likely to diffuse. An oxidation process in this state caused increasing oxidation of metal of W~~-ete~~. and Si~~. And~~, and expansion of volume occurred. Therefore, difference of stress occurred between polysilicon and metallic silicide in the lower portion of the metallic silicide layer. A ~~And,~~ difference of stress also occurred between the metallic silicide and SiN layer in the upper portion of metallic silicide layer. As a result, fastening between the metallic silicide layer and SiN deteriorated~~. And~~, and peeling off of the SiN layer occurred.

[0009] That is, according to the method mentioned above, a gate electrode 40 comprising polysilicon layer 42, metallic silicide layer 43,and SiN layer 44 was formed. When ~~And, when~~ its surface was observed, the state of the surface shown in Fig.5(b) was recognized. In Fig.5(b), metallic silicide crystal 45 grew like notches in the horizontal direction, because the side wall of gate electrode 40 was abnormally oxidized. In addition~~And~~, SiN layer 44 was likely to peel off

due ~~owing~~ to abnormal oxidation as mentioned above.

[0010] As a method of preventing abnormal oxidation mentioned above, a method of implanting nitrogen in the side wall of gate electrode 40 has been suggested (c.f. JP 08-321613).

[0011] However, the conventional method has a problem in that voids (vacancies) occur~~red~~ because of nitrogen implanted in the semiconductor substrate.

SUMMARY OF THE INVENTION

[0012] Therefore, the present invention is aimed at providing a method of manufacturing semiconductor substrate which can restrain the occurrence of abnormal oxidation under heat treatment at a high temperature after forming a metallic silicide layer.

[0013] The problem mentioned above can be solved~~,~~ because the present invention includes the following. First, a ~~comprises as next.~~

~~The first is a~~ method of manufacturing a semiconductor element ~~comprising:~~ includes:

~~a process of~~ forming a gate electrode having a metallic silicide layer on a semiconductor substrate,

~~a process of~~ decreasing grain boundaries on the surface of the metallic silicide at least at a portion ~~of~~ which is exposed, and

~~a process of~~ forming a spacer consisting of oxide film on the side wall of the gate electrode.

[0014] Second, in ~~The second is~~ a method of manufacturing a semiconductor element according to the first method, ~~wherein~~ the process of decreasing the ~~said~~ grain boundaries is a process of performing heat treatment to the ~~said~~ metallic silicide layer in an atmosphere consisting of a chief element of nitrogen gas.

[0015] Third, in ~~The third is~~ a method of manufacturing a semiconductor element according to the first method, ~~wherein~~ the process of decreasing the ~~said~~ grain boundaries is a process of performing heat treatment to the ~~said~~ metallic silicide layer in an atmosphere consisting of a chief element of argon gas.

[0016] Fourth, in ~~The fourth is~~ a method of manufacturing a semiconductor element according to the first method, ~~wherein~~ the process of decreasing the ~~said~~ grain boundaries is a process of performing heat treatment to the ~~said~~ metallic silicide layer in an atmosphere consisting of a mixture gas of chief elements of nitrogen and ammonia.

[0017] Fifth, in ~~The fifth is~~ a method of manufacturing a semiconductor element according to the first method, ~~wherein~~ the process of decreasing the ~~said~~ grain boundaries is performed after performing a reduced pressure process.

[0018] These methods include ~~has~~ a process of decreasing grain boundaries after forming a metallic silicide layer. Therefore~~So~~, occurrence of abnormal oxidation in the side wall of the gate electrode can be restrained, even if a process of treatment at high temperature is performed after the process of decreasing grain boundaries.

[0019] Here, the process of decreasing grain boundaries means a process of performing heat treatment to the metallic silicide layer, at least a portion of which is exposed in an atmosphere of inoxidizable gas consisting ~~consisted~~ of a chief element of nitrogen, argon, or mixture gas of nitrogen and ammonia.

[0020] Moreover, for example, a chief element of nitrogen means an atmosphere including more than 99% density of nitrogen gas. Especially, it means an ~~a state of~~ atmosphere including less than 100ppm of oxidizable gas (oxygen gas etc.). Incidentally, other inoxidizable gas can be included if the gas mentioned above is a chief element and the density of oxidizable gas is less

than 100ppm.

BRIEF DESCRIPTION OF THE DRAWINGS

[0021] Figs. 1(a) to (d) are sectional views of a semiconductor element in the process of an Embodiment of the present invention.

[0022] Fig. 2 is a plan view of the gate electrode formed by the method of the present invention.

[0023] Fig. 3 is a sectional view of the gate electrode formed by the method of Embodiment 2 of the present invention.

[0024] Figs. 4(a) and (b) are sectional views of a NMOS-FET having an LDD structure manufactured by the method of the present invention.

[0025] Fig. 5(a) is a sectional view of a gate electrode formed by the conventional art, and Fig. 5(b) shows a state of abnormal oxidation of gate electrode.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0026] Hereafter, Embodiments 1 to 4 of the method of manufacturing a semiconductor element according to present invention will be described, referring to the drawings.

<Embodiment 1>

[0027] ~~The~~ Embodiment 1 of the manufacturing method of the present invention comprises a process of forming a gate electrode having a metallic silicide layer on a semiconductor substrate, a process of performing heat treatment of the ~~said~~ metallic silicide layer (at least a portion of which is exposed)~~,~~ in a gas atmosphere consisting of a chief element of nitrogen (a heat treatment process of metallic silicide layer), and a process of forming spacers

comprising oxide films on the side walls of the ~~said~~ gate electrode; in this order.

[0028] At ~~In the concrete, at~~ first, an isolation of an element is performed, as shown in Fig. 1(a), by a ~~the~~ method which is the same as the conventional method known in public. After isolating an element, a gate oxide film 1 and a polysilicon layer 2 are formed, as shown in Fig. 1(b), by a ~~the~~ method known ~~shown~~ in public. Then, an ion implantation is performed so as to introduce an impurity to the polysilicon layer 2 to make an electrode from it. In addition~~And~~, a metallic silicide layer 3 is formed on the polysilicon layer 2 by a PVD method or a CVD method. ~~:~~ Here, the temperature for forming the metallic silicide layer 3 is preferably 400° C to 600° C. After forming the metallic silicide layer 3, a heat treatment at a ~~which~~ temperature ~~is~~ higher than that for forming the metallic silicide layer 3 is performed. Here, the temperature of this heat treatment is preferably 700° C to 800° C.

[0029] Incidentally, the manner ~~way~~ of heat treatment is not limited at all. The ~~However, the~~ heat treatment can be performed together with a process of forming an SiN layer 4, which becomes a hard mask for forming a gate and a mask for making self-aligned contact, on the top of the gate electrode.

[0030] On ~~In~~ this occasion, the SiN layer 4 is preferably formed by a CVD method of reduced pressure, which can make a minute film with little H included. The heat treatment by this CVD with reduced pressure is performed at a temperature higher than the temperature for forming the metallic silicide layer 3.

[0031] After forming the SiN layer 4, a photolithography for forming a gate electrode 5 is performed, as shown in Fig. 1(c), and ~~. And~~, an etching for forming a gate (process of forming the gate electrode) is performed. By this gate etching, the side walls of the portions of metallic silicide layer 3 are exposed.

[0032] After forming the gate electrode 5, ~~it gets~~ a heat treatment (process of

heat treatment of the metallic silicide layer) is performed. This is performed in a gas atmosphere including nitrogen as a chief element, in a chamber of heat treating apparatus (RTA) purged with nitrogen, for example.

[0033] The temperature of heat treatment in the heat treatment process of the metallic silicide layer is preferably 700 to 800° C in a view point of decreasing grain boundaries of silicide crystal without fail. The process time is preferably 30 to 40 sec. in the same point of view.

[0034] Since the gas atmosphere in the chamber consists of a chief element of nitrogen, the gas atmosphere consists of little oxidizable gas. That is, the density of oxidizable gas in the atmosphere is less than 100 ppm. Therefore, diffusion of oxygen in the metallic silicide layer 3 is contained, and. ~~And~~, abnormal oxidation can be prevented. Moreover, the grain boundary of the silicide crystal in the side wall ~~becomes less~~ decreases. Therefore~~So~~, diffusion of oxygen or moisture after forming the gate can be prevented.

[0035] Moreover, nitrogen gas is convenient for manufacturing devices, because it is ~~not expensive and~~ easy to use and not expensive.

[0036] After performing heat treatment in the process of treating the metallic silicide layer with heat, an oxidizing treatment is performed in a common furnace. By performing this oxidizing treatment, as shown in Fig. 1(d), spacers comprising oxide film 10, 10 are formed on the side walls of the polysilicon layer and tungsten silicide layer, and on the gate oxide film. Incidentally, these spacers are used as a mask layer for forming an LDD (Lightly Doped Drain) structure, and as a protection layer for protecting the side walls of the gate electrode.

[0037] In the heat treatment mentioned above, the atmosphere for performing the heat treatment can include either oxygen or oxygen with moisture, because diffusion of oxidizing substance in the metallic silicide layer is restrained. Moreover, in order to obtain a preferable thickness of an oxide film, the

atmosphere, process temperature, process time, gas flow quantity etc. can be set voluntarily.

[0038] Fig. 2 shows a ~~state of~~ top surface of the gate electrode 5 formed by the manufacturing method of Embodiment 1. In Fig. 2, what is formed vertically in the central portion of the figure is the gate electrode 5. Moreover, what is formed at each side of the gate electrode 5 is the gate oxide film. As apparently shown in Fig. 2, abnormal oxidation resulting in deposition of notched crystal described referring to Fig. 5(b) does not come out on the side walls of gate electrode 5. That is, by the manufacturing method of the present invention, the side wall of the gate electrode is oxidized uniformly without any abnormal oxidization.

[0039] As described above, according to the manufacturing method of Embodiment 1, abnormal oxidation can be prevented when the side wall is oxidized after forming the gate electrode, in any condition such as atmosphere (only oxygen or with moisture), process temperature, process time, gas flow quantity etc.

<Embodiment 2>

[0040] The manufacturing method of Embodiment 2 of the present invention comprises a process of forming a gas electrode having a metallic silicide layer on a semiconductor substrate, a process of performing heat treatment of the metallic silicide layer, at least a portion of which is exposed in an atmosphere consisting of a chief element of argon gas, and a process of forming spacers comprising an oxide film on each side of the gate electrode; in this order.

[0041] The manufacturing method of Embodiment 2 is the same as the manufacturing method of Embodiment 1 except for the process of treating the metallic silicide layer with heat. The ~~; wherein the~~ chief element of the gas atmosphere for heat-treatment is not nitrogen, but argon.

[0042] After ~~That is, after~~ forming a gate electrode 5 as well as the manufacturing method of Embodiment 1, heat-treatment in an atmosphere of a chief element of argon gas is performed in a chamber of a heat-treating apparatus (RTA) purged with argon gas. Here, the chief element of argon gas means that the density of argon in the gas atmosphere is not less than 99%, and. ~~And~~, especially, the density of oxidizable gas (oxygen gas etc.) is not more than 100 ppm.

[0043] In an atmosphere of a chief element of argon gas, abnormal oxidation can be prevented as well as nitrogen gas. Moreover, a method of ~~by~~ using argon gas of Embodiment 2 is profitable ~~in the occasion~~ when nitrization of a source region or a drain region of the semiconductor substrate must be avoided.

[0044] Incidentally, the process temperature, the process time etc. of the heat-treatment condition is the same as the manufacturing method of Embodiment 1.

[0045] In addition~~And~~, spacers comprising an oxide film are ~~is~~ formed on the side wall of the gate electrode as in ~~same as~~ Embodiment 1, after performing a heat-treating process of the metallic silicide layer, which is performed in the argon gas atmosphere of the chief element.

<Embodiment 3>

[0046] The manufacturing method of Embodiment 3 comprises a process of forming a gate electrode having a metallic silicide layer on a semiconductor substrate, a process of performing heat-treatment in an atmosphere of a chief element of a mixture gas consisting of nitrogen and ammonia, and a process of forming spacers comprising an oxide film on the side wall of the gate electrode; in this order.

[0047] The method of Embodiment 3 is the same as Embodiment 1 except the heat-treating process of the metallic silicide layer. The ~~, wherein the~~

heat-treatment in a gas atmosphere of the chief element is not nitrogen but a mixture gas of nitrogen and ammonia.

[0048] At first, a gate electrode 5 is formed as in ~~same as~~ Embodiment 1. After this, a chamber is purged with nitrogen gas so as to make the density of oxidizable gas less than 100 ppm. Subsequently, the wafer is placed ~~let~~ in the chamber of the heating apparatus so as to heat it with a lamp.

[0049] In the meantime, the wafer is heated up to a prescribed temperature. Then, ammonia gas is introduced into the chamber. And, an atmosphere of mixture gas consisting of nitrogen and ammonia is made. Then, a heat-treatment is made. The temperature in this occasion is preferably not less than 650° C, and. ~~And,~~ it is still preferable if it is 700 to 800° C.

[0050] The density of ammonia gas in the atmosphere is preferable if it is 1 to 3%, provided that the nitrified region mentioned later is formed in a reasonable range.

[0051] Spacers ~~And, spacers~~ comprising an oxide film are ~~is~~ formed on the side wall of the gate electrode as in ~~same as~~ Embodiment 1, after performing the heat-treating process on the ~~of~~ metallic silicide layer, which is performed in the atmosphere of mixture gas of chief elements of nitrogen and ammonia.

[0052] According to the method of Embodiment 3, abnormal oxidation on the side wall does not occur. As ~~And, as~~ shown in Fig. 3, nitrified region 7 is formed in a range of the side wall to the bottom portion of metallic silicide layer 3 assisted by the ammonia gas. Therefore, nitrogen of high density is introduced into the oxide film on the substrate except the portion under gate electrode 5. As a result, diffusion of impurities from the substrate to the spacers formed on the side wall of gate electrode 5 can be prevented.

[0053] After performing heat-treatment mentioned above, oxidizing treatment is performed in a common oxidizing furnace as in ~~same as~~ Embodiment 1. The gas ~~let~~ in the furnace as an atmosphere in this occasion preferably consists of a

chief element of nitrogen. In the meantime, the furnace is heated up to a preferable temperature. Subsequently, a gas for oxidizing is introduced there.

[0054] This gas may consist of oxygen or moisture.

<Embodiment 4>

[0055] The method of Embodiment 4 of the present invention comprises a process of forming a gate electrode having a metallic silicide layer on a semiconductor substrate, a process of performing heat-treatment of the metallic silicide layer, at least a portion of which is exposed in an atmosphere of a chief element of nitrogen gas (heat-treating process of metallic silicide layer), and a process of forming spacers comprising an oxide film on the side wall of the gate electrode; in this order. The ~~; wherein the~~ heat-treating process of metallic silicide layer is performed after a process of performing a reduced pressure treatment (reduced pressure treating process).

[0056] At ~~In the concrete, at~~ first, etching for forming the gate is performed as in ~~same as~~ Embodiment 1. After etching to form the ~~for~~ gate, the photoresist used for etching is removed, and. ~~And,~~ a gate electrode is formed. After this, the reduced pressure treating process is performed by using a low pressure CVD device, for example. Subsequently, a heat-treatment in an atmosphere of a chief element of nitrogen gas is performed as in ~~same as~~ Embodiment 1.

[0057] The reduced pressure treatment is performed by taking the semiconductor substrate forming ~~formed~~ the gate electrode in the furnace at its temperature of less than 550° C.

[0058] By performing the reduced pressure treatment, the density of oxygen on the surface of the wafer (density of oxidizable gas) can be made less than 100 ppm.

[0059] After performing the reduced pressure process, the wafer is heated up. Heat ~~And, heat~~ treatment in an atmosphere of a chief element of nitrogen gas

at 700 to 800° C is performed as in ~~same as~~ Embodiment 1 (heat treating process of the metallic silicide layer).

[0060] In this occasion, if the wafer is heated up without performing the reduced pressure process, abnormal oxidation occurs, because the density of oxygen between wafers is high.

[0061] The pressure of the reduced pressure process is preferably 13 to 65Pa.

[0062] After performing heat treatment at ~~of~~ more than 650° C, the wafer is cooled down to the process temperature or inletting temperature. Then, the wafer is taken out. After this, a spacer comprising an oxide film is formed on the side wall of the gate electrode as in ~~same as~~ Embodiment 1.

[0063] According to Embodiment 4, the density of the oxidizable gas is efficiently decreased. Moreover, the heat treating process of metallic silicide layer after the reduced pressure process can be performed in processing apparatus, which can process a batch of wafers. Therefore, productivity can increase.

[0064] Next, an example of the manufacturing method of a NMOS-FET having an LDD structure is described referring to Fig. 1 and Fig. 4.

[0065] At first, as mentioned before in the description with reference to Fig. 1(a) to Fig. 1(c), gate electrode 5 (generally polysilicon) is formed on the semiconductor substrate 1. Next, as shown in Fig. 4(a), phosphorus is introduced by ion implantation using the gate electrode 5 as a mask. By this, shallow n^- layer 50 is formed all over the source and drain region of semiconductor substrate 1.

[0066] After this, as shown in Fig. 4(b), an oxide film 10 (side wall) is formed on the side wall of gate electrode 5.

[0067] This oxide film 10 is formed with the condition mentioned before (condition described in Embodiments 1 to 4). By this, the gate electrode with restrained ~~restraining~~ abnormal oxidation can be formed.

[0068] After forming oxide film 10, arsenic is introduced by ion implantation using oxide film 10 and gate electrode 5 as a mask. By this, deep n^+ layer 70 is formed on ~~in~~ the portion of the source and drain region distant from the gate electrode 5. After this, wiring etc. is performed. Then, NMOS-FET of LDD structure is manufactured.

[0069] Incidentally, the manufacturing method mentioned above is not only applied to NMOS-FET, but is also applied to various semiconductor elements such as CMOS-FET etc.

[0070] And, the present invention is not limited to Embodiments 1 to 4.

[0071] For example, the material of the metallic silicide layer is not limited to

[0072] Tungsten silicide, which is preferable in practical use. That is, molybdenum silicide or titanium silicide etc. is available.

[0073] Moreover, if the heat treatment after forming the metallic silicide layer is performed at a temperature higher than the temperature of forming the metallic silicide, an SiN layer formed by a reduced pressure CVD method is not always necessary.

ABSTRACT OF THE DISCLOSURE

A method of manufacturing a semiconductor device includes ~~invented comprises~~ a process of forming a gate electrode ~~(5)~~ having a metallic silicide layer ~~(3)~~ on a semiconductor substrate, a process of decreasing boundaries of grains on the surface of the ~~said~~ metallic silicide layer, ~~(3)~~ at least a portion of which is exposed, and a process of forming spacers comprising an oxide film ~~(10)~~ on the side wall of the ~~said~~ gate electrode ~~(5)~~; in this order. Thus, ~~so as to avoid the~~ abnormal oxidation of the ~~said~~ metallic silicide layer ~~(3)~~ is avoided.